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PATENT
1152-0263P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicants:	Hideaki SAKAGUCHI	Conf.:	4601
Appln. No.:	09/624,014	Group:	2857
Filed:	July 21, 2000	Examiner:	Mary C. BARAN

1/27 MSH

For: TESTING DEVICE AND TESTING METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUITS

AMENDMENT UNDER 37 C.F.R. § 1.111

Assistant Commissioner for Patents
Washington, D.C. 20231

January 8, 2003

Sir:

In reply to the Examiner's Office Action dated September 11, 2002, the period for response having been extended one (1) month to January 11, 2003, the following amendments and remarks are respectfully submitted in connection with the above-identified application.

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 10, line 21, bridging page 11, line 1, with the following rewritten paragraph:

9 1

--a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the